Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY
Winter Examination-2015

Subject Name: Semiconductor Memories Design

Subject Code: 5TE03SMD1 Branch: M.Tech (VLSI and Embedded Systems Design)

Semester: 3 Date: 22/12/2015 Time: 2:30 To 5:30 Marks: 70

Instructions:

(1) Use of Programmable calculator and any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

SECTION – I

Q-1 **Attempt the Following questions** **(07)**

a. Define static noise margin.
b. What is scaling of SRAM?
c. Define Redundancy in SRAM Design.
d. What is importance of Sense Amplifier in SRAM?
e. What are the disadvantages of 4T-SRAM Cell with Polysilicon Resistor Load?
f. What are differences between 6T SRAM cell and 4T Loadless SRAM Cell?
g. What is the function of Pre-charge circuit in SRAM?

Q-2 **Attempt all questions** **(14)**

(a) Explain the Moore's Law of semiconductor memories.
(b) Draw and explain the Six-Transistor (6T) CMOS SRAM Cell.

OR

Q-2 **Attempt all questions** **(14)**

(a) Draw and explain the Four-Transistor (4T) Loadless SRAM Cell.
(b) Draw and explain the typical circuit with a current-mirror type sense amplifier, a PRL SRAM cell and precharge/load transistors.

Q-3 **Attempt all questions** **(14)**

(a) Explain with the help of block diagram Delay-Line Based Timing Control method used in SRAMs.
(b) Draw and explain the circuit diagram of the 4-1 pass-transistor column decoder with a predecoder.

OR

Q-3 **Attempt all questions** **(14)**

(a) Explain with the help of circuit diagram the Address Transition Detector (ATD).
(b) Explain with the help of block diagram Replica-Loop Based Timing Control

method used in SRAMs.

SECTION – II

Q-4 **Attempt the Following questions** **(07)**

a. What is latency time of DRAM?
b. What do you mean by refresh cycle?
c. What is digitline pitch?
d. What is wordine pitch?
e. What is rate of activation?
f. What are the disadvantages of open digitline array architecture?
g. What are the advantages of folded digitline array architecture?

Q-5 **Attempt all questions** **(14)**

(a) Draw and explain 3-transistor DRAM cell.
(b) Write a note on Multiple Memory Arrays.

OR

Q-5 **Attempt all questions** **(14)**

(a) Draw and explain the functional block diagram of 1K-bit DRAM.
(b) Enlist the Modes of operation of DRAM. Explain with the help of timing diagram Page Mode.

Q-6 **Attempt all questions** **(14)**

(a) What is the importance of Equilibration and Bias Circuits in DRAM? Explain.
(b) Draw and explain Bilevel Digitline Array Architecture Schematic.

OR

Q-6 **Attempt all Questions** **(14)**

(a) Draw and explain basic circuit of Nsense and Psense Amplifiers.
(b) Draw and explain the basic circuit of Bootstrap Wordline Driver.