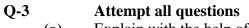
	Enrolln	ment No:		No:	
			AH UNIVER Examination-		
	Subject	t Name: Semiconductor Men	nories Design		
	Subject	t Code: 5TE03SMD1	Branch: M.Tech (VLSI a	and Embedded Systems Desig	gn)
	Semeste	er: 3 Date: 22/12/2015	Time: 2:30 To 5:30	Marks: 70	
	(2) (3)	tions: Use of Programmable calcula Instructions written on main a Draw neat diagrams and figur Assume suitable data if neede	answer book are strictly to res (if necessary) at right p	be obeyed.	
Q-1	a. b. c. d. e. f. g.	What is scaling of SRAM?  Define Redundancy in SRA	M Design. e Amplifier in SRAM? of 4T-SRAM Cell with Poen 6T SRAM cell and 4T I	· ·	(07)
Q-2	(a) (b)	Attempt all questions Explain the Moore's Law of Draw and explain the Six-Tr			(14)
			OR		
Q-2	(a) (b)	Attempt all questions Draw and explain the Four-Tournament of the properties of the	al circuit with a current-m		(14)
Q-3	(a)	Attempt all questions Explain with the help of method used in SRAMs.	block diagram Delay-L	ine Based Timing Control	(14)
	<b>(b)</b>	Draw and explain the circuit with a predecoder.	it diagram of the 4-1 pas  OR	s-transistor column decoder	



**(14)** 

- (a) Explain with the help of circuit diagram the Address Transition Detector (ATD).
- (b) Explain with the help of block diagram Replica-Loop Based Timing Control Page 1 | | 2



		SECTION – II		
Q-4	Attempt the Following questions			
	a.	What is latency time of DRAM?		
	b.	What do you mean by refresh cycle?		
	c.	What is digitline pitch?		
	d.	What is wordine pitch?		
	e.	What is rate of activation?		
	f.	What are the disadvantages of open digitline array architecture?		
	g.	What are the advantages of folded digitline array architecture?		
Q-5		Attempt all questions		
	(a)	Draw and explain 3-transistor DRAM cell.	(14)	
	<b>(b)</b>	Write a note on Multiple Memory Arrays.		
		OR		
Q-5		Attempt all questions		
	(a)	Draw and explain the functional block diagram of 1K-bit DRAM.		
	<b>(b)</b>	Enlist the Modes of operation of DRAM. Explain with the help of timing diagram Page Mode.		
Q-6		Attempt all questions		
	(a)	What is the importance of Equilibration and Bias Circuits in DRAM? Explain.	(14)	
	<b>(b)</b>	Draw and explain Bilevel Digitline Array Architecture Schematic.		
		OR		
<b>Q-6</b>		Attempt all Questions		
	(a)	Draw and explain basic circuit of Nsense and Psense Amplifiers.		
	<b>(b)</b>	Draw and explain the basic circuit of Bootstrap Wordline Driver.		

